

CLAIMS

1. A dynamic repeater comprising:
 an input gate including an input transistor
 having an input node and two or more clocked input gates
~~operative to place the repeater in a pre-charge mode in~~
~~response to a first clock signal and to place the repeater~~
~~in an evaluate mode in response to a second clock signal;~~
 and
 an output node operative to output a voltage of
 $V_{cc}/2$ in response to a voltage of $V_{cc}/2$ on the input node
 in the evaluate mode.

2. The repeater of claim 1, wherein the clocked
 transistors include a PMOS transistor coupled to V_{cc} and an
 NMOS transistor coupled to V_{ss} , the input transistor being
 connected between said PMOS and NMOS transistors.

3. The repeater of claim 1, further comprising:
 an intermediate node coupled to one of a source
 and a drain of the input transistor;
 an output inverter having an output coupled to
 the output node and an input coupled to the intermediate
 node;

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a second transistor connected in series with the first transistor, said second transistor having one of a source and a drain connected to a voltage supply.

4. The repeater of claim 3, wherein the output inverter has a noise margin of about $V_{cc}/2$.

5. The repeater of claim 3, further comprising a feedback inverter having an input coupled to the intermediate node and an output coupled to a gate of the second transistor.

6. The repeater of claim 5, wherein the output inverter and feedback inverter each have a noise margin of about $V_{CC}/2$.

7. The repeater of claim 3, wherein the first and second transistors comprise PMOS transistors, wherein the reference voltage is V_{cc} , and wherein the input transistor is an NMOS transistor.

8. The repeater of claim 7, wherein the repeater is operative to latch a LOW signal on the intermediate node

during the evaluate mode in response to receiving a HIGH data signal at the input node.

9. The repeater of claim 3, wherein the first and second transistors comprise NMOS transistors, wherein the reference voltage is V_{ss} , and wherein the input transistor is an PMOS transistor.

10. The repeater of claim 9, wherein the repeater is operative to latch a HIGH signal on the intermediate node during the evaluate mode in response to receiving a LOW data signal at the input node.

11. A dynamic bus comprising:

a plurality of bus lines, each bus line including

a dynamic driver at an input,

a clocked flip flop at an output,

a plurality of inverting stages connected

between the driver and the flip flop, and

a dynamic repeater connected between two of said inverting stages, said dynamic repeater having a noise margin of $V_{cc}/2$.

15. The bus of claim 14, wherein the driver is operative to switch between the pre-charge mode and the evaluate mode in response to a first clock signal and the

17. The bus of claim 16, wherein the driver is operative to switch between the pre-charge mode and the evaluate mode in response to a first clock signal and the repeater is operative to switch between the pre-charge mode and the evaluate mode in response to the first clock signal.